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ANNA UNIVERSITY (CEG/MIT CAMPUSES)

B.E. /B.Tech / B. Arch (Full Time) - END SEMESTER EXAMINATIONS, NOV / DEC 2024

ELECTRONICS AND COMMUNICATION ENGINEERING

Semester-III

EC23C02 ANALOG CIRCUITS DESIGN

Time:3hrs (Regulation2023) **Max.Marks: 100**

CO1	Choose appropriate biasing circuits for BJT and MOSFET discrete amplifiers
CO2	Design and analyze single stage and multistage BJT amplifiers
CO3	Analyze the characteristic of MOSFET amplifiers, the effect of source and load
CO4	Analyze the high frequency response of BJT and MOSFET amplifiers
CO5	Design and analyze IC MOSFET amplifiers

BL – Bloom's Taxonomy Levels

(L1-Remembering, L2-Understanding, L3-Applying, L4-Analysing, L5-Evaluating, L6-Creating)

PART- A(10x2=20Marks)

(Answer all Questions)

Q.No.	Questions	Marks	CO	BL
1	For the circuit shown in Fig.1 Determine R_B such that V_{CEQ}=2.5V. Assume $\beta(h_{fe})$=100 and V_{BEon}=0.7V.	2	1	2
2	What is the Role of C_C and R_E in Voltage divider biasing circuit	2	1	1
3	Determine the input resistance for the circuit shown in Fig.2. The circuit is biased with I_{CQ}=1mA and assume $\beta(h_{fe})$=100 and V_{BEon}=0.7V.	2	2	2
4	The transistor parameters are $h_{fe} = \beta = 100$ and $V_A = 120V$. Determine its output resistance shown in the Figure-3	2	2	3
5	For the circuit in Figure 4 , the transistor parameters are $V_{TN} = 0.6$ V and $\mu nCox(W/L) = 400\ \mu A/V^2$. Determine V_D	2	3	3
6	Consider R_1 and R_2 as equal value resistors. Determine the value of approximate voltage gain if R_D=2kΩ and λ=0 (Vide Figure-5)	2	3	3
7	Consider the coupling capacitance $C_C = 2\mu F$ shown in Figure-6 and determine the lower cutoff frequency. The transistor parameters are $V_{TN} = 0.4$ V, $\mu nCox(W/L) = 200\mu A/V^2$, and $\lambda = 0$.	2	4	4
8	A bipolar transistor has parameters $\beta o(h_{fe}) = 120$, $C\mu = 0.02pF$, and $f_\beta = 90MHz$ and is biased at $I_{CQ} = 0.2mA$. Determine $C\pi$	2	4	2
9	Determine the output resistance of cascade current mirror shown in the Figure-7	2	5	2
10	List the properties of current mirror.	2	5	1

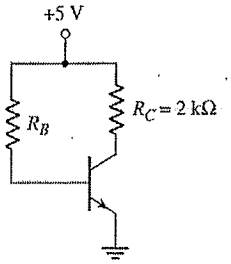


Figure-1

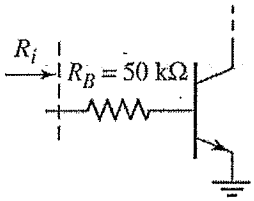


Figure-2

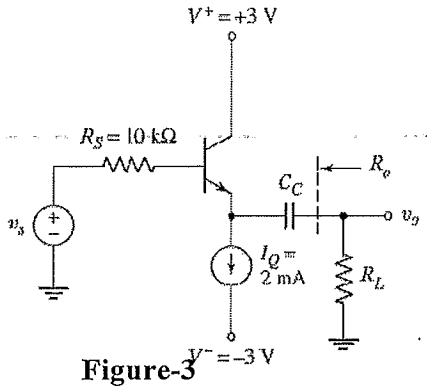


Figure-3

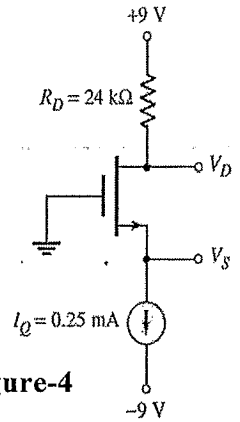
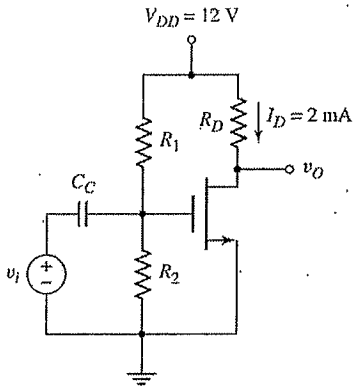


Figure-4



Figure=5

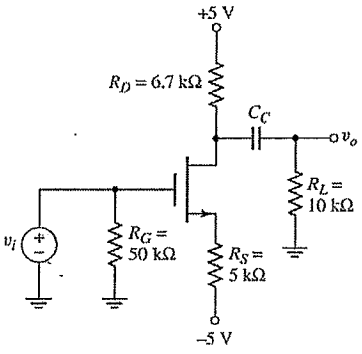


Figure-6

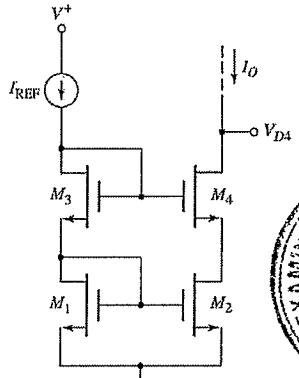


Figure-7

PART- B(5x 13=65Marks)

Q.No.	Questions	Marks	CO	BL
11 (a)	Derive the stability factors due to change in I_{CBO}, h_{fe} (β) and V_{BE} for the circuits shown in below Figure-8	13)	1	5
	OR			
11 (b)	The nominal transistor parameter are shown in Figure- 9, $V_{TP} = -2$ V, $V_{DD} = 5$V, $V_{SS} = -5$V, $R_1 = 300$ kΩ, $R_2 = 100$ kΩ, $R_D = 2$ kΩ, $R_S = 3$kΩ, μ pCox(W/L) =1mA/V^2. Calculate V_{SG}, I_D and V_{SD}.	13)	1	4
12 (a)	For the circuit shown in Figure-10. Assume the transistor parameters are: $V_{EB(ON)} = 0.7$V, β(h_{fe})=100 and $V_A = 100$V. (a) Find small-signal current gain Ai = io/is and the (b) input impedance R_{ib}, & output impedance seen by collector (c) Also determine the maximum symmetrical output voltage swing.	13)	2	4
	OR			
12 (b)(i)	Derive the overall current gain and input resistance of the Darlington pair circuit shown in Figure-11.	(7)	2	5
	Consider the cascode circuit in the Figure -12,Let V_{CC} =12V and R_L =1kΩ, hfe = β = 150. (a) Design the circuit such that V_{CE1} = V_{CE2} =3V, V_{RE} =1V. I_{CQ1} = I_{CQ2} =2mA and neglect the base-currents. Assume a current flow through the biasing network is 0.1 I_{CQ}. (b) Determine the small-signal voltage gain, Av = vo/ vs . (d) Determine the small signal input impedance and output impedance.	(6)	2	4

13 (a)	The transistor in the Figure-13, is biased with a constant current source. The transistor parameters as: $V_{TN} = 2$ V, $\mu nCox(W/L) = 4.8$ mA/V^2, and $\lambda = 0.01$ V^{-1}. The load resistor is $R_L = 4$ kΩ. (a) Determine the value of output resistance Ro, when I = 0.8 mA. (b) Determine its current gain and input impedance (c) Determine the maximum output voltage swing produced by the circuit.	13	3	4
	OR			
13 (b)	Consider the PMOS common-gate circuit in Figure-14. The transistor parameters are: $V_{TP} = -1$V, $\mu p\ Cox(W/L) = 1$ mA/V^2, and $\lambda = 0.01$V^{-1}. (x) Determine R_S and R_D such that $I_{DQ} = 0.75$ mA and $V_{SDQ} = 6$ V. (y) Determine the input impedance R_i and the output impedance R_o. (z) Determine the load current *io* and the output voltage *vo*, if $i_i = 5 \sin \omega t\ \mu$A.	13	3	4
14 (a)	Determine the (a) upper cut-off frequency for the circuit shown in Figure-15 , Assume gm =4mS,Cgs =47fF and Cgd =7.4fF . (b) Find C_G, C_D and C_S for f_L=100Hz	13	4	5
	OR			
14 (b)	For the amplifier shown in the below Figure-16 a) Draw its high frequency small signal equivalent circuit and derive the expression for the upper cutoff frequency of current gain io/is. b) Consider the circuit parameters as $R_C = R_L = 4$ kΩ, $r\pi = 2.6$ kΩ, $R_1 \| R_2 = 200$ kΩ, $C\pi = 0.8$ pF, $C\mu = 0.05$ pF, and gm = 38.5 mA/V. Determine the cutoff frequency f_T and 3dB frequency cutoff frequency f_β of the transistor. c) Find the lower cutoff frequency when C_{C1}, C_{C2} and C_E=1μF	13	4	5
15 (a)	Derive the expressions for input voltage, output voltage, systematic offset error and output resistance of the Wilson Current Source	13	5	1
	OR			
15 (b)	Consider the MOSFET amplifier with active load shown in Fig-17 (a) Find Point A and B locations and I_{DQ}. (b) Output voltage when V_{IN} =1V (c) Find small-signal voltage gain, input impedance, output impedance. Assume $V_{TN} = 0.7$ V, $\|V_{TP}\| = 0.65$ V, $\mu n\ Cox = 250\mu$A/V^2, $\mu p\ Cox = 80\mu$A/V^2, (W/L) n =40, (W/L) p =45, $\lambda n = \lambda p = 0.02$ V^{-1}. Assume I_{bias} =0.5 mA, V_{DD} =1.8 V	13	5	5

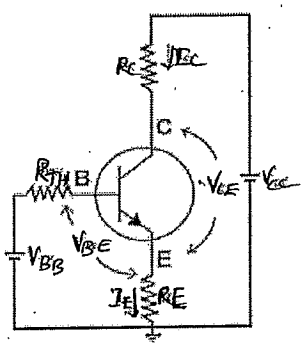


Figure-8

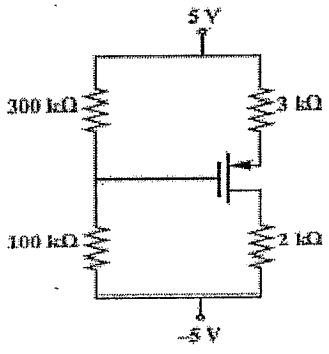


Figure-9

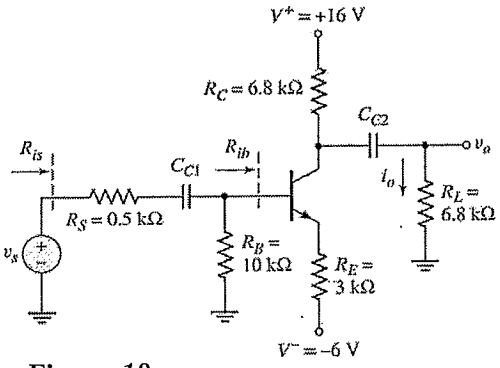


Figure-10

PART- C(1x 15=15Marks)

Q.No.	Questions	Marks	CO	BL
16.	For the circuit in Figure-18, the transistor parameters are: μn Cox(W/L) =1 mA/V2, V_{TN}= 2 V, and $\lambda = 0.01V^{-1}$. (a) Determine the maximum value of C_L such that the bandwidth is at least BW = 5 MHz.	11	4	6
b)	Derive common mode rejection ratio of BJT differential amplifier with resistive load. How to improve the common-mode rejection ratio	4	2	2

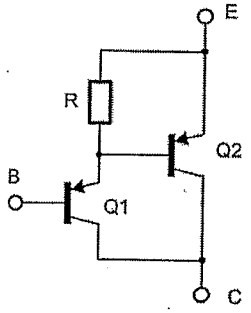


Figure-11

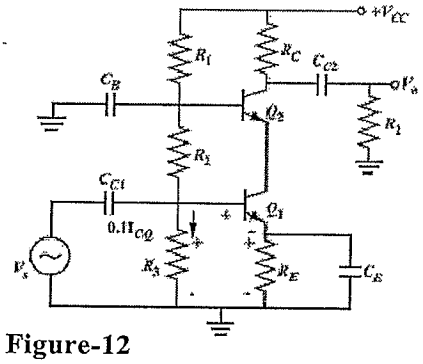


Figure-12

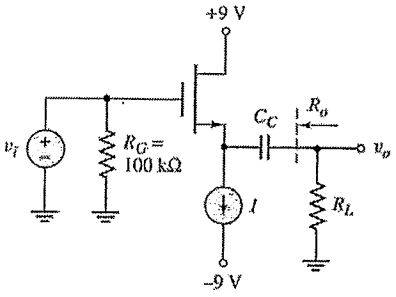


Figure-13

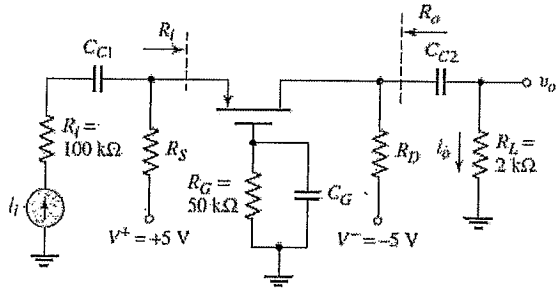


Figure-14

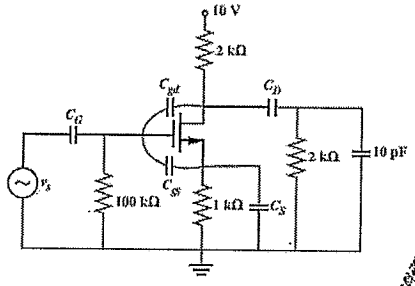


Figure-15

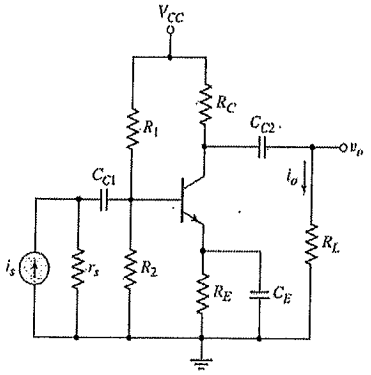


Figure-16

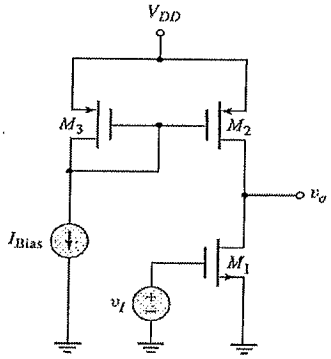


Figure-17

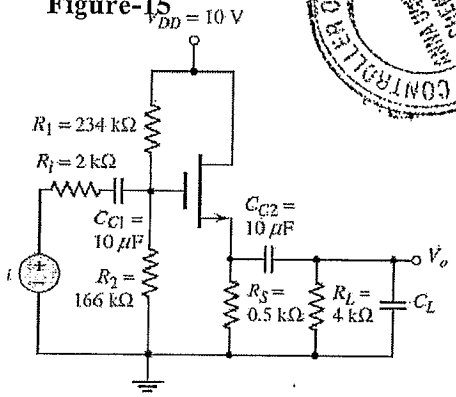


Figure-18